

...We are boundary-scan.



WWW.JTAG.COM

datasheet *Production Systems*

Stand-alone production system

Production integration systems (DLL, LV, LW, TS, VB, .NET and EXE)

Symphony and OEM systems

...We are boundary-scan.

Features

- Broad set of production alternatives for stand-alone and integrated operation
- Execution of all JTAG Technologies boundary-scan applications developed on ProVision or 'Classic' platforms
- Player for SVF, JAM and STAPL files from third-party sources
- Results collection for analysis at repair station
- Built-in report generator and ticket printing facility
- Password-protected entry levels
- Support for all popular National Instruments' platforms
- Support for Microsoft Visual Basic, C, C++, and .NET
- Fault analysis to pin-level via BSD (Boundary-Scan Diagnostics) and JTAG Visualizer
- Open architecture - links can be provided to virtually all third-party ATE systems.

Overview of boundary-scan

The JTAG Technologies product line is focused on testing printed circuit boards (PCBs) and systems and includes on-board device programming features, all utilizing powerful JTAG boundary-scan technology. Boundary-scan compliance to IEEE 1149.1 and related standards overcomes the physical access limitations associated with advanced integrated circuit packaging such as ball-grid arrays (BGAs).

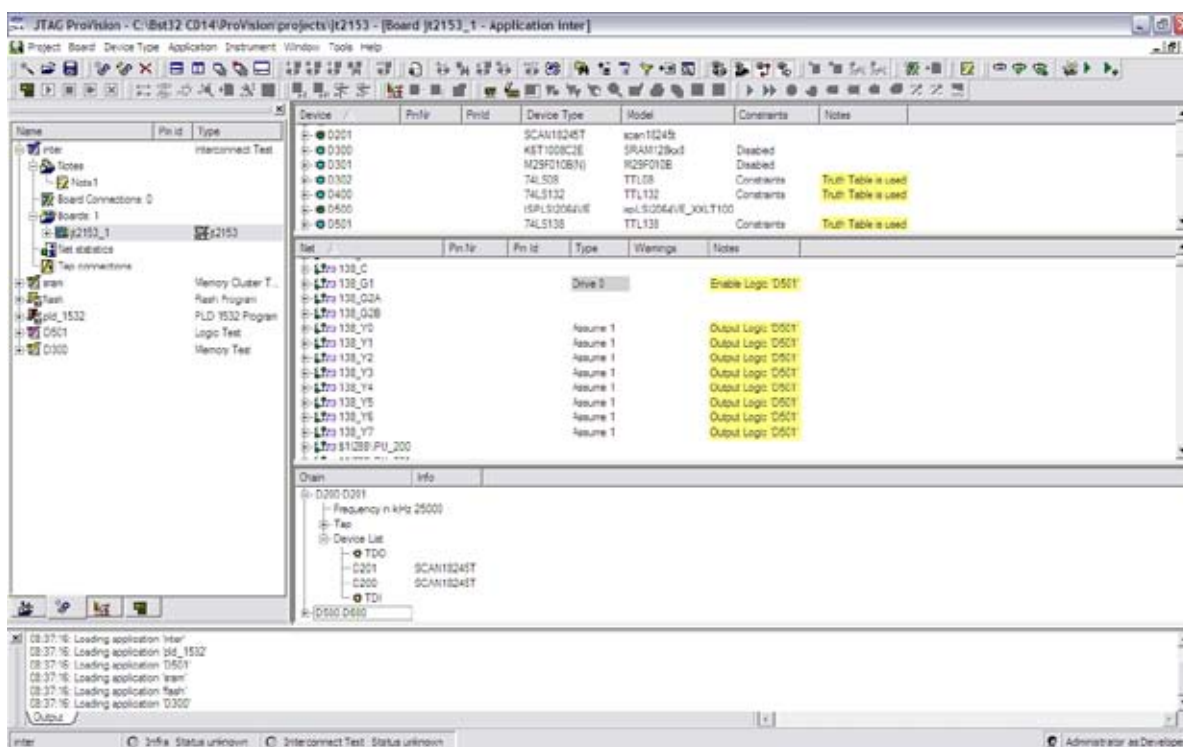


In addition, boundary-scan can simplify test fixtures and product handling when compared to conventional test and programming methods such as in-circuit (bed-of-nails) testing and off-line device programming. JTAG Technologies tools are ideal for prototype hardware debugging and device programming, production testing and in-system programming (ISP) and field service.

Application development and validation

Boundary-scan applications are typically prepared and validated by test engineering teams or individuals using the highly automated JTAG Technologies ProVision development tool (Figure 1) or the prior generation known as JTAG Classic. Both environments provide great flexibility in the generation of test applications for scan path infrastructure testing, interconnect testing, cluster and memory block testing, functional logic testing plus programming of devices such as flash memories, serial PROMs, CPLDs and embedded flash within micro-controllers. DFT (Design-For-Test) fault coverage

Figure 1, JTAG Technologies ProVision



analysis is an important capability of the development tools guiding designers and test engineers in achieving fault coverage goals. Analysis results can be viewed graphically using JTAG Visualizer in both schematic and layout domains. Refer to companion brochures on ProVision and Visualizer for more detailed information.

All test and ISP applications can be executed and validated in the development environment prior to delivery to the production facility. Test sequences can also be created for production testing and / or programming within the ProVision development tool. Complete production test archives can then be exported from ProVision including the previously prepared sequence.

Test results are presented to the designer in a truth-table format that highlights all differences from the expected response. An optional diagnostics tool analyzes the test results and indicates the location of the fault or faults; JTAG Visualizer presents the fault identification right on the schematic and layout drawings.

Choices for production

A wide variety of execution (run-time) software is available to meet different requirements. Often, a stand-alone boundary-scan solution will be preferred for prototype debugging and for field service as well as in some production scenarios. The choice of a stand-alone boundary-scan strategy allows the manufacturer to separate the task of structural testing (and associated fault diagnostics) from subsequent functional tests. Moreover, a stand-alone system might be used for repetitive and possibly time-consuming programming of flash memories and/or PLDs to 'unload' a more expensive in-circuit tester.

In other cases, rather than establishing a stand-alone station, it may be desirable to combine boundary-scan with an existing test system such as an in-circuit (bed-of-nails) tester, flying probe system, or functional test system. Among the benefits of combining boundary-scan with other test methods are:

- Achieving more comprehensive test coverage, taking advantage of the particular strengths of the various techniques
- Reduced product handling by combining test steps into one station
- Reduced operator training, by including the boundary-scan control and results collection within the test plan of the existing test system

- Reduced test fixture complexity and minimized duplication/ overlap of test boundaries.

A wide variety of integration choices is available, grouped in three classifications:

- Production Integration Packages (PIP), typically used by functional test system builders
- Symphony systems, consisting of all of the software and hardware modules needed to upgrade an existing ICT or flying probe system to full JTAG Technologies boundary-scan capability
- OEM systems, devised by and available from third-party tester vendors, which incorporate JTAG Technologies software and hardware modules

Stand-Alone Boundary-scan Station

Stand-alone boundary-scan operations may be performed on a dedicated test system running JTAG Technologies Production Stand-Alone (PSA) software featuring AEX Manager -a graphical JTAG application executive program.

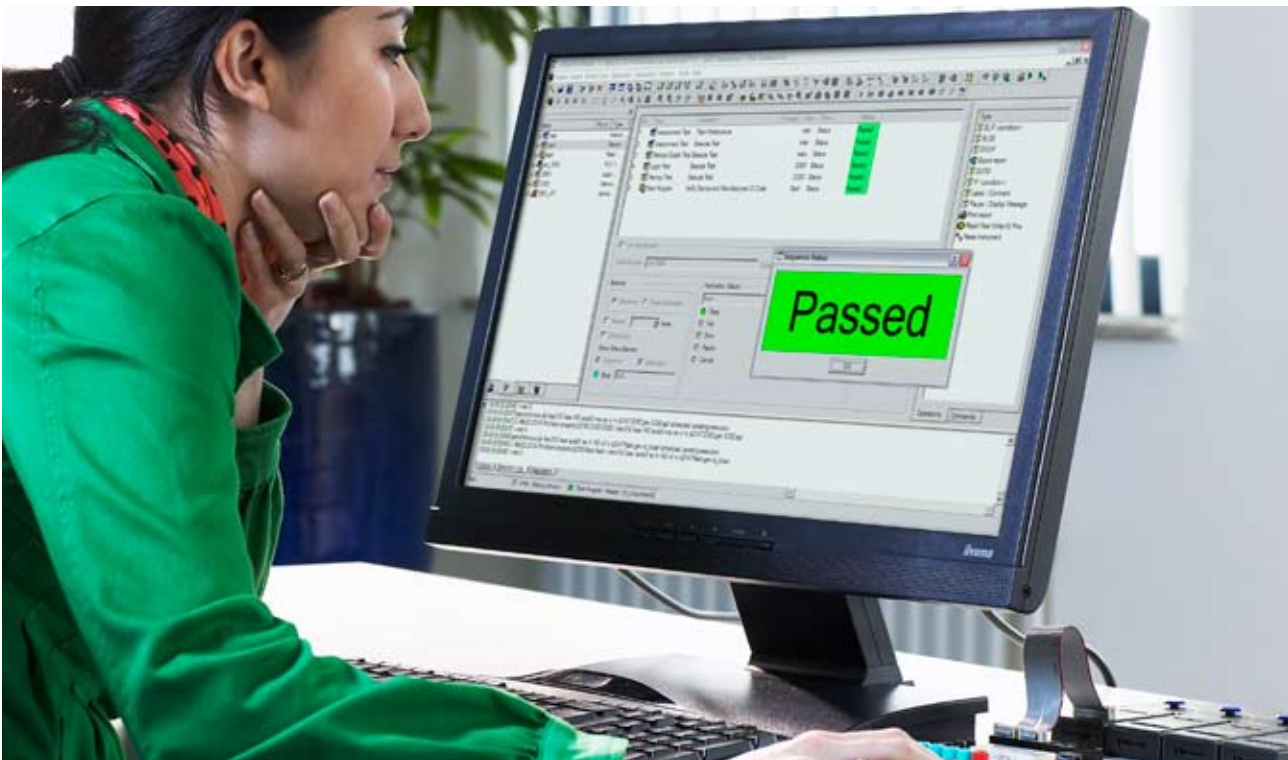
PSA supports all of the boundary-scan hardware controllers from JTAG Technologies and handles up to four targets simultaneously depending on the controller type. Multiple boundary-scan controllers can be used from a single licence for even greater throughput.

JTAG Technologies PSA package provides the runtime control and management functions through the embedded AEX Manager. Features include If-Then-Else conditional branching, test flow control, test report generation and results logging recorded by serial number.

A variant of the AEX Manager is also embedded within JTAG ProVision, the application generation tools suite. Thus ProVision software not only allows generation, compilation and execution of individual applications, but also the generation of application 'scripts' or 'sequences'.

Complete, validated boundary-scan application scripts can then be confidently exported to production facilities by designers or test engineering professionals.

Alternatively, a single instance of JTAG ProVision can be used effectively for both development and production, providing a cost-effective solution in cases where both activities are to be performed at the same station.

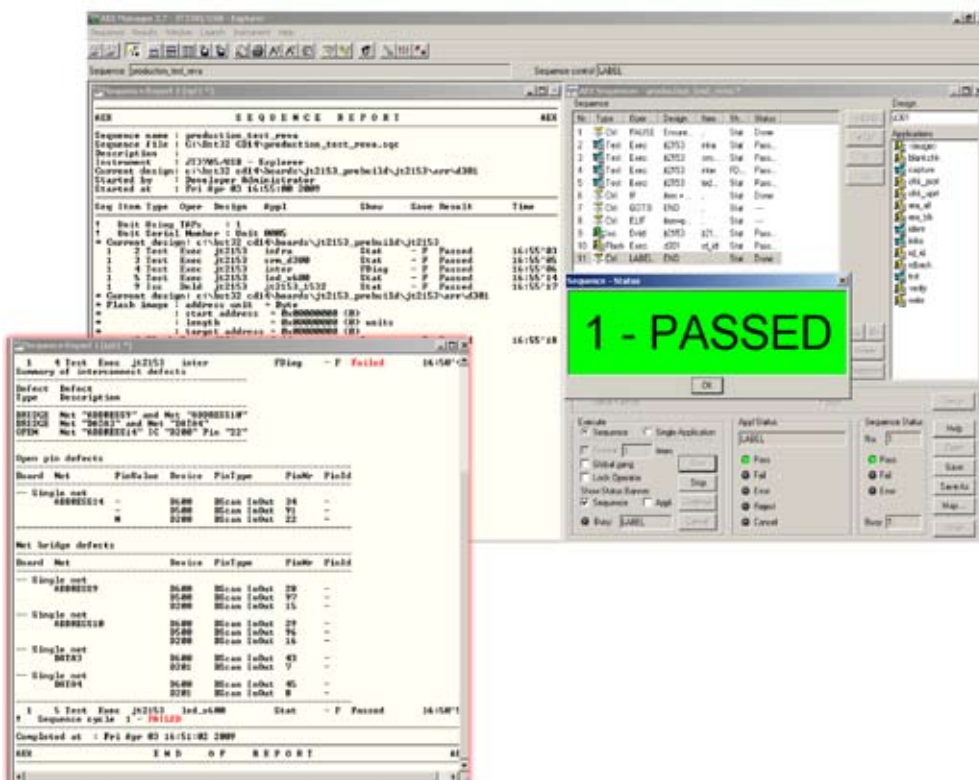


The production stand-alone software package (PSA) and the alternate ProVision platform implementation, include runtime software (execution modules) and AEX Manager with its graphical user interface. All production operations required for testing, flash programming, and CPLD programming using IEEE 1532, JEDEC, SVF or JAM / STAPL formats can be executed.

To support different types of user activities in the production environment, AEX contains three password-protected levels:

- Developer Full access to all features allowing the test engineer to create and validate sequences
- Engineer Used by the production supervisor to view the progress of a sequence execution or to change operational settings

Figure 4, AEX Manager Sequence Screen with a BSD report



- Operator Used by the operator to initiate execution of the production sequence, perform tasks defined in the sequence, and observe the results

The results of a boundary-scan application sequence are presented in three levels of detail:

- Pass/fail display, suitable if the technician is not expected to troubleshoot the board, but rather to send defects to the repair department.
- Truth-table format, as shown in Figure 3, in which differences between actual and expected response are highlighted, allowing the user to quickly focus on problem resolution. The user can filter the results to see only the failing vectors and/or nets.
- Full diagnostic output, provided by the boundary-scan diagnostic (BSD) software module, which pin-points the fault causes and corrective action. Figure 4 is an example of the AEX manager with the corresponding BSD output screen.

During sequence execution, results data are stored in a predefined location associated with the particular target board for subsequent use in repair. In addition to the built-in data storage and logging capabilities of the stand-alone production package, the AEX Manager contains a default interface to the widely used Teradyne TRACS database management system.

Production Integration Packages

JTAG Technologies production integration packages (PIPs) support execution of boundary-scan applications in a range of software environments such as those from National Instruments and Microsoft. The PIPs are often employed to run boundary-scan testing and programming within a functional test system.

Supported platforms are:

- PIP / TS for National Instruments TestStand
- PIP / LV for National Instruments LabVIEW
- PIP / LW for National Instruments LabWindows
- PIP / ATE for Geotest ATEasy
- PIP / VB for Microsoft VisualBasic
- PIP / DLL for Microsoft C and C++
- PIP / Net for Microsoft .NET
- PIP / EXE for general integration via system calls

Each PIP with the exception of PIP / EXE includes an API for the associated software environment and is supported by a comprehensive manual including examples for each library within the PIP package.

Language-based PIPs (PIP / DLL, PIP / VB, PIP / LW and PIP / Net) are used by experienced developers to add boundary-scan functions into their test executive programs. PIP / TS and PIP / LV offer high-level execution via custom step-types and virtual instruments, respectively; see Figure 5 for a LabVIEW example.

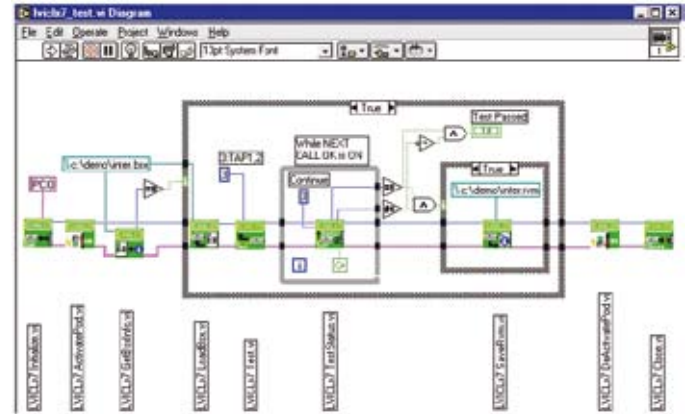


Figure 5, Example test program using PIP for LabVIEW

PIP/EXE utilizes an executive program or a batch file to launch DOS-like command lines with appropriate command line options. The reference manual included with this system fully documents the command line operations.

JTAG Structural Tester Integration

JTAG Technologies' structural test integration packages add powerful boundary-scan features to existing in-circuit and flying probe structural test systems, often at lower cost than native vendor options. Furthermore, off-line test generation and debug reduce the load on costly ATE systems and allows swift implementation of boundary-scan on many of today's ATE platforms.

All boundary-scan integration options require that a JTAG-compatible (IEEE Std 1149.x) hardware controller be implemented within the system. Solutions that employ a JTAG Technologies controller are ideal for high-speed in-system flash programming as well as testing. Solutions which use a controller native to the in-circuit tester or flying probe system are suitable for boundary-scan testing but not for flash programming. Symphony systems from JTAG Technologies provide complete integration solutions for a range of popular in-circuit testers and flying probe systems:

- Symphony 3070 for the Agilent 3070 in-circuit test system Integration with the Agilent 3070 uses the JTAG Technologies JT 37x7/ APC controller incorporating a full-function

DataBlaster controller, QuadPod signal conditioning unit and isolating relays conveniently packaged for installation in a standard Agilent pin-driver card slot.

Alternatively, for bench-top applications, a JT 37x7/TSI controller may be used with options for USB 2.0 and Ethernet interfaces. The TSI allows connection to an HP workstation or PC without sacrificing a valuable PCI card slot. Symphony 3070 supports legacy HP-UX and MS Windows-based 3070 testers with easy migration from UNIX to PC.

- Symphony 3030 for the SPEA 3030 in-circuit test system.
- Symphony 4040 for the SPEA 4040 flying probe system including the JT 3727/TSI boundary-scan controller.
- Symphony 228x for the Teradyne 228x and TS12x TestStation in-circuit testers may be based on the native Teradyne DSM hardware or on JTAG Technologies

JT 37x7 DataBlaster hardware. When a JTAG Technologies boundary-scan controller is used, its output is passed to the fixture via JT 2147 Custom Function Modules, two of which can be mounted on a Teradyne Custom Function Board. The CFM provides isolation of power and ground between the JTAG Technologies controller and the ICT system.

- Symphony APT-9000 for the Takaya 9400 flying probe system uses a JT 37x7 controller powered by the 9400 to execute boundary-scan applications. TAP signals are connected via the four flying probes or an edge connector within the shuttle connection system.
- Symphony 1240 for the Hioki 1240 flying probe system uses JTAG Technologies hardware to execute boundary-scan applications. The JT 37x7 controller is powered by the 1240.

Table A summarizes the Symphony systems and controllers that are included.

Table A: Symphony systems

| Product name | Vendor and system type | JTAG Technologies controller | Native hardware |
|-------------------|--|--|---|
| Symphony 228x | Teradyne 228x (GenRad) and TestStation ICT | JT 37x7 / TSI (including JT 2147 / CFM) if flash programming is required | Teradyne DSM if flash programming is not required |
| Symphony 3070 | Agilent 3070 ICT | JT 37x7 / APC | N/A |
| Symphony 1240 | Hioki 1240 FPT | JT 37x7 / TSI | N/A |
| Symphony APT 9000 | Takaya 9400 FPT | JT 37x7 / TSI | N/A |
| Symphony 3030 | SPEA 3030 ICT | JT 37x7 / TSI | N/A |
| Symphony 4040 | SPEA 4040 FPT | JT 37x7 / TSI | N/A |

In addition to the Symphony systems supplied and supported by JTAG Technologies, our OEM partners offer the following integration options for their test systems:

Aeroflex 42xx series and 5800 in-circuit test systems. Only hardware; JT 2147/ AGP. Contains isolation to separate signals from Aeroflex test system.

DigitalTest MTS500 Condor flying probe system and MTS300 Sigma in-circuit tester
 Seica S40 Pilot flying probe system

Table B summarizes the controller options for the OEM integration solutions. Please contact the respective vendors for details on their current product offerings.

Table B: OEM systems

| Vendor and system type | JTAG Technologies controller | Native hardware |
|------------------------------------|---|--|
| Aeroflex 42xx ICT | JT 37x7 / PCI | N/A |
| Aeroflex 5800 combinational tester | JT 37x7 / PXI | N/A |
| DigitalTest Condor | JT 37x7 / TSI optional if flash programming is required | Use DigitalTest MFC if flash programming is not required |
| Seica Pilot FPT | JT 37x7 / TSI | N/A |

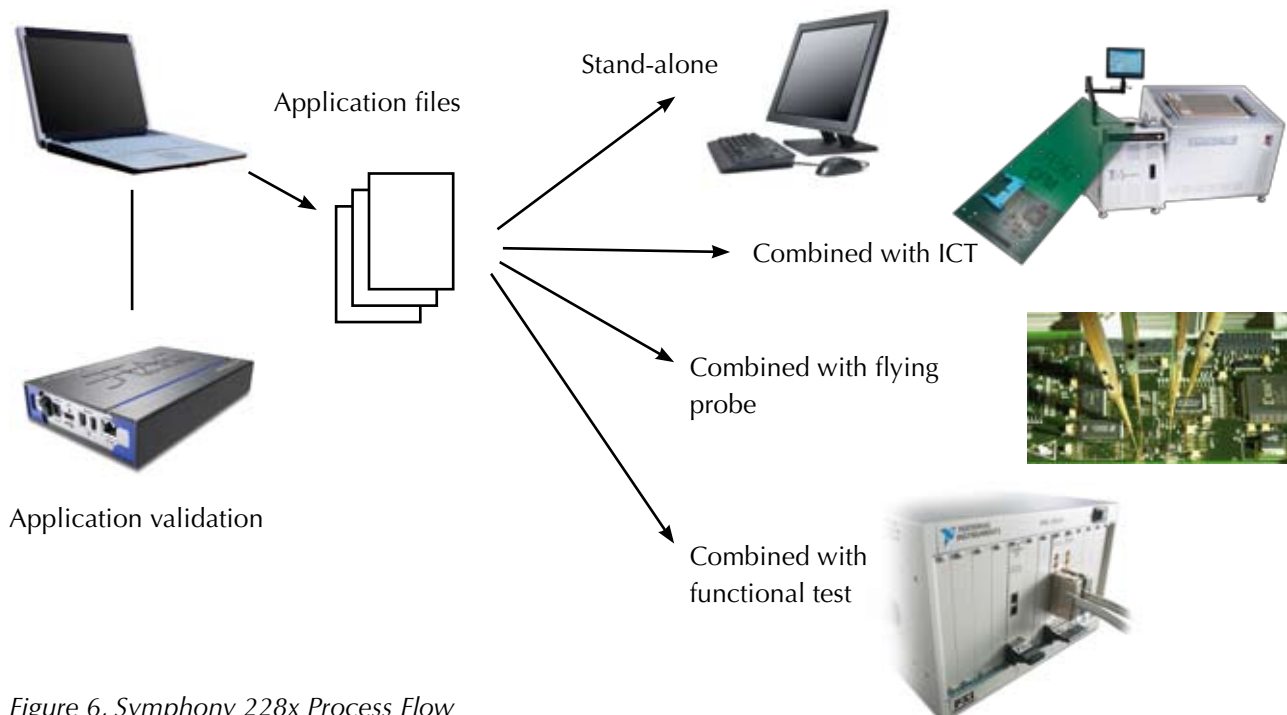


Figure 6, Symphony 228x Process Flow

Production systems using JTAG Technologies controllers run the applications directly, as generated by ProVision or Classic. System documentation guides the user on the best method to call the applications from the host executive system. For systems using existing ATE resources, rather than a JTAG Technologies controller, an alternative test formatting process is required in which the applications are recompiled for the specific controller type.

Special processing, results collecting, is also required on test results obtained using the native hardware for analysis by JTAG Technologies boundary-scan diagnostics tools. (See Figure 6 for the implementation flow for either system option).

Diagnostics and repair

Optional Boundary-Scan Diagnostic (BSD) software is used with any of the production stand-alone or production integration packages and with any of the JTAG Technologies boundary-scan controllers. BSD is also included as a standard component in all Symphony packages. BSD interprets the test results and identifies the fault causes on the target via easily-read

English language text messages. An example BSD output is shown in Figure 7.

Diagnostics and corrective action are provided for all types of manufacturing faults including multiple faults: stuck-at-1, stuck-at-0, opens, shorts and incorrect ICs. A user-defined fault dictionary can also be used to support cluster tests, diagnosing stuck-at faults within the cluster. BSD analyzes multiple faults in a single pass of the test sequence, resolving them into separate, single fault causes. No extra tests, such as adaptive diagnostics, are needed to produce repair information, saving valuable time in the troubleshooting process. A significant benefit of BSD is its ability to handle multiple boundary-scan chains within the target system, offering advantages of improved execution times and flexible circuit partitioning.

The diagnostic output can also be viewed graphically by means of JTAG Visualizer. Using Visualizer, the repair person quickly finds all instances of faulty net(s) within the schematic and board layout by clicking on the net name or pin number in the diagnostic report. As shown in Figure 8, the operator may choose to see both views at the same time in different windows. Visualizer's zoom function shows the fault location in greater detail, and by selecting a specific device or pin on a device, the properties of the device or pin can be displayed. The user customizes the color settings for rapid identification of fault classes such as opens, bridges, stuck-at-1, stuck-at-0, and defective ICs. Further detail on JTAG Visualizer is provided in a separate brochure.

| Defects | Net(s) | Board | Net | Device | Pin Type | Pin No | Pin Id | | |
|----------|---------------------|---------|-----------|---------|--------------|--------|--------------|----|------|
| Open pin | 0200-22 | J2152_1 | ADDRESS8 | 0300 | BScan In-Out | 15 | E208 | | |
| Bridge | ADDRESS19,ADDRESS1E | J2152_1 | ADDRESS10 | 0300 | Addr | 12 | A3 | | |
| | | | | 0301 | Addr | 12 | A3 | | |
| | | | | 0500 | BScan In-Out | 37 | Bip64 | | |
| | | | | 0400 | BScan In-Out | 28 | Bip01 | | |
| | | | | J2152_1 | ADDRESS10 | 0300 | BScan In-Out | 16 | F211 |
| | | | | 0300 | Addr | 31 | A10 | | |
| | | | | 0301 | Addr | 31 | A10 | | |
| | | | | 0500 | BScan In-Out | 36 | Bip63 | | |
| | | | | 0400 | BScan In-Out | 29 | Bip10 | | |

Figure 7, typical BSD report

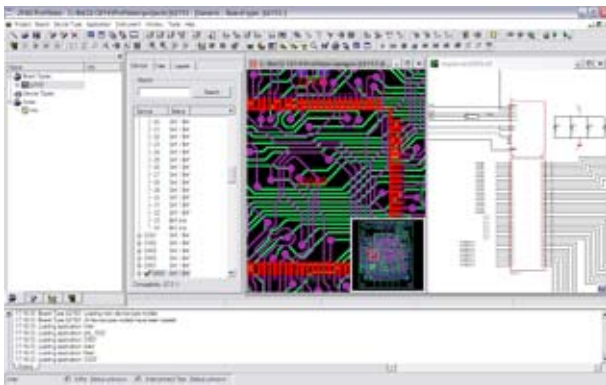


Figure 8, Visualizer fault display on schematic and layout drawings

Ordering information

| Product | Description |
|----------------------|---|
| PSA | Stand-Alone Production Package consisting of AEX Manager and run-time test and programming modules |
| ProV_PL / A / N or F | JTAG ProVision execution and compilation platform used for development and production on the same station (node-locked or floating license) |
| PIP/xyz | Production Integration Packages for custom integration applications (xyz = DLL, VB, TS, LV, LW, ATE, EXE, NET) |
| PM 3790 | Pin-level Boundary-Scan Test Diagnostics |
| Symphony 3030 | Integration package for SPEA 3030 tester |
| Symphony 4040 | Integration package for SPEA 4040 tester |
| Symphony 228x | Integration package for Teradyne 228x & TestStation tester |
| Symphony 228x Plus | Integration package for Teradyne 228x & TestStation tester |
| Symphony 3070 | Integration package for Agilent 3070 series tester |
| Symphony 9400 | Integration package for Takaya APT 94xx series tester |
| Symphony 1240 | Integration package for Hioki flying probe tester |

| Hardware | Controllers & accessories |
|------------------------|---|
| JT 37x7 / TSI | DataBlaster with triple-serial interface (Ethernet, FireWire and USB 2.0) and JT2147 QuadPod |
| JT 37x7 / APC | DataBlaster in Agilent Pin Card format with integral isolation relays (supplied with Symphony 3070) |
| JT 2147 / 10 | TAP Pod system with JT 2148/10 QuadPod Transceiver and 4 x JT2149 TAP pods |
| JT 2147 / 13 | Industrial QuadPod with 4 x JT2149 TAP pods and cable splitter |
| JT 2147 / CFM | Custom Function Module (one TAP interface) |
| JT 2147 / AGP | QuadPod for Aeroflex 42xx GP card (supports four TAPs) |
| JT 2149 | QuadPod TAP pod |
| JT 3705 / USB Explorer | 2-TAP Basic USB controller |

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